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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MICHAEL A. LAMSON ET AL

Serial No. 09/631,198 (TI-28674)

Filed August 3, 2000

For: STRUCTURE AND METHOD OF HIGH PERFORMANCE
TWO LAYER BALL GRID ARRAY SUBSTRATE

Art Unit 2814

Examiner Dilinh P.Nguyen

Customer No. 23494

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3-26-04

Jay M. Cantor

Jay M. Cantor, Reg. No. 19,906

DECLARATION OF JAY M. CANTOR

Jay M. Cantor declares as follows:

That he is a registered patent attorney, Reg. No. 19906.

That he is an attorney of record in the subject application.

That, on information and belief, the attached Patent Disclosure TI28674 was reduced to practice by a computer model of the design concept as shown in the drawing attached thereto prior to December 31, 1998.

That, on information and belief, the attached Patent Disclosure TI28674 was submitted to the Texas Instruments Incorporated invention review committee and was approved for filing prior to December 31, 1998.

That the TI28674 Patent Disclosure meets the definition of "invention" as stated by
the United States Supreme Court in Pfaff v Wells Electronics, 525 U.S. 55 (U.S. 1998).

I declare under penalty of perjury that the above facts and opinion true and
correct..

3-26-04
Date



Jay M. Cantor

-MSG MF= UU6994JZ FR=MURG TO: S#
S#=153 ST=C DIV=0009 CC=00074 BY=AGKG AT= 08:57 AM

TO: Michael A. Lamson MIKL
Navinchandra Kalidas NCK

FROM: Agatha Gutierrez AGKG

SUBJECT: TI-28674 - HIGH FREQUENCY SEMICONDUCTOR DEVICE PACKAGE

The above-referenced patent disclosure was reviewed by the Assembly/
Test/Packaging (ATP) Committee on 3/29/04. This disclosure was
Authorized for Filing.

If you have any questions about this decision, or if you think the
wrong decision may have been made, please let me know.

Regards,

Mark A. Valetti
ATP Patent Counsel
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ATP Patent Committee Administrator
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1352
MAV

Patent Disclosure TI28674
High Frequency Semiconductor Device Package

MAR 29 2004

As clock frequencies and current levels increase in semiconductor devices, the packaging designs are challenged to provide acceptable signal transmission and stable power and ground supplies. Providing stable power is usually achieved by using multiple planes in the package, properly coupled to one another and to the signal traces. Indeed, the signal traces must be coupled to the return current paths in the ground or power architecture to ensure the most efficient power and signal transmission.

In many devices independent power sources are needed for core operation and for output buffer supply but with a common ground source.

Costs of the packaging system must kept at a minimum while providing the required performance. Many times this means providing a minimum set of planes and signal layers in the package.

This disclosure describes a package conductor layout for a high frequency and high performance digital signal processor (DSP) chip using a two layer package design. The package layout for the signal and power layer is shown in Figure 1 for the right hand quadrant only. A ground plane covers a second layer below the layer shown.

The wide tracks in each of the four corners are the power supply paths for the core region of the chip. These are a very wide traces to allow maximum coupling to the ground plane layer below to minimize inductance. These traces are connected to the smaller rectangular core power plane in the center that is coupled the ground plane below and provides a platform to connect the core power vias to the chip. The core power vias are located sequentially between the ground vias to promote coupling and reduce the effective inductance in the via paths.

The wider traces shown along the side of the package provide buffer power to the chip and are interspersed among the narrower signal traces shown. The location and extra width of the buffer power traces promoting greater coupling to the ground plane and also the signal traces to minimize the effective inductance of the buffer power paths.

The narrow signal traces have a controlled width and are uniformly coupled to the ground plane allowing a constant impedance relation to ground. This is important for efficient high frequency power transmission on the signal traces.

Computer models of this design concept were evaluated for electrical performance on

It is planned to use this package design on the low cost C6X device.

Mike Lamson



**Two Layer BGA Package
For High Frequency DSP Device**

